VC30F Program Data Sheet

Official version: 1.0.3
Publish date: 2023-02-09

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catalogs

1 Products

1.1 summarize

The VC30F is a health monitoring sensor chip with built-in PD and integrates 3 physical channels and 2 adjustable logic channels. It supports high-precision exercise heart rate (HR) and static blood oxygen saturation (SPO2) monitoring functions, and features ultra-low power consumption and live body recognition, making it suitable for smartwatches, smart bracelets and other wearable smart devices.

1.2 functional block diagram

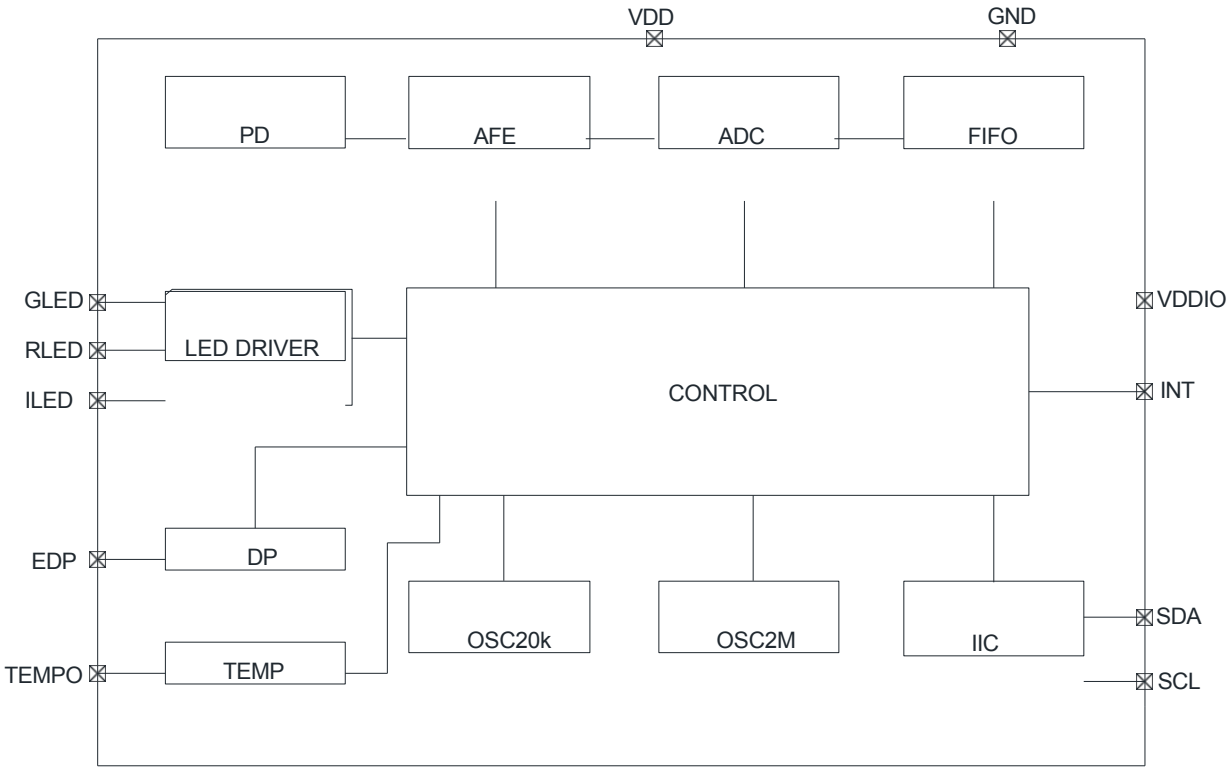


Figure 1-1 VC30F Function Block Diagram

1.3 specificities

- **ultra-low power**
  - Typical power consumption in heart rate mode 80μA @ 25Hz including LED illumination power consumption
  - Typical Power Consumption in Oxygen Mode 500μA @ 25Hz including LED illumination power consumption
  - Unworn power consumption: ~10μA @1Hz
  - Sleep current: ~400nA
- **Chip Built-in Functions**
  - automatic dimming
  - Automatic wear detection
  - Temperature Detection
- **LED Drive Current**
  - 1.25mA~160mA
- **Internal FIFO**
  - 128Bytes
- **communications interface**
  - IIC clock support up to 1MHz
  - IIC7-bit device address is 0x33
- **Key Electrical Characteristics**
  - VDD:3.0V~3.6V
  - VDDIO: 1.8V~3.6V
- **seal inside**
  - OLGA Package
  - Size:2.3mm*2.5mm*0.6mm,12PIN
- **Typical applications that can be supported**
  - pulse rate
  - oximetry
  - Wear detection
- **Algorithm footprint**
  - Space for heart rate algorithm: 25Hz: 1.6kRAM, 9.8kROM
  - Space for blood oxygen algorithm: 25Hz: 2.1kRAM, 6.4kROM

2 Technical indicators

2.1 Limiting electrical parameters

Table 2-1 VC30F Limit Electrical Parameters

parameters	minimum value	maximum values	unit (of measure)
VDD	0	3.6	V
VDDIO	0	3.6	V
operating temperature	-30	80	℃

*Note:

- Exceeding the limiting operating conditions may cause permanent damage to the chip;
- To ensure that the chip is in normal working condition for a long time, please do not operate the chip under the limit parameters, otherwise the reliability of the chip will be affected.

2.2 Recommended working conditions

Table 2-2 Recommended Working Conditions

parameters	Conditions/notes	minimum value	typical value	maximum values	unit (of measure)
VDD	AFE Power Supply	3.0	3.3	3.6	V
VDDIO	I/O Power Supply	1.8	3.3	3.6	V

2.3 timing parameter

2.3.1 IIC Timing Parameters

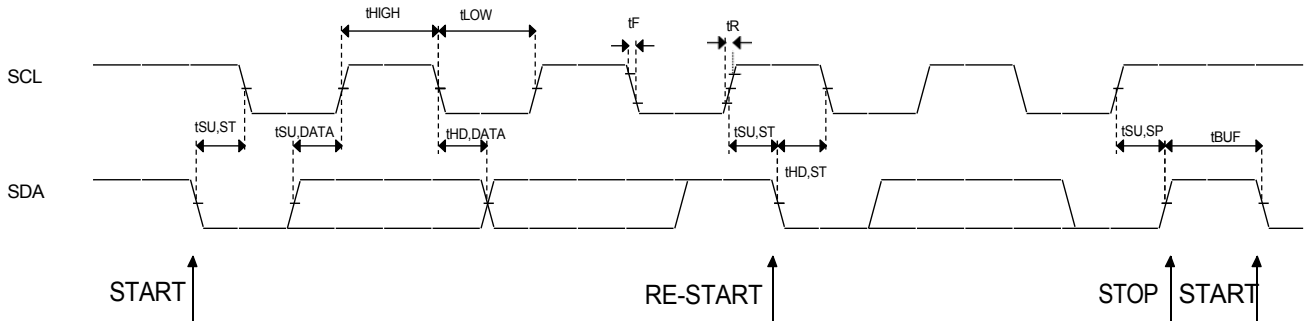


Figure 2-1 IIC

Timing Diagram

parameters	notation	minimum value	maximum values	unit (of measure)	prerequisite
clock frequency	fSCL	-	100		normal mode
		-	400		High Speed Mode
		-	1000		Ultra High Speed Mode
Clock Low Level Time	tLOW	4.7	-		normal mode
		1.3	-		High Speed Mode
		0.5	-		Ultra High Speed Mode
Clock High Time	tHIGH	4.0	-		normal mode
		0.6	-		High Speed Mode
		0.26	-		Ultra High Speed Mode
rising time	tR	-	1000		normal mode
		-	300		High Speed Mode
		-	120		Ultra High Speed Mode
		-	300		normal mode

Parameters

parameters	notation	minimum value	maximum values	unit (of measure)	prerequisite
Start condition hold time	tHD,STA	4.0	-	µs	normal mode
		0.6	-		High Speed Mode
		0.26	-		Ultra High Speed Mode
Stop condition establishment time	tSU.STO	4.0	-	µs	normal mode
		0.6	-		High Speed Mode
		0.26	-		Ultra High Speed Mode
Bus Idle Time	tBUF	4.7	-	µs	normal mode
		1.3	-		High Speed Mode
		0.5	-		Ultra High Speed Mode
Data setup time	tSU,DATA	250	-	ns	normal mode
		100	-		High Speed Mode
		50	-		Ultra High Speed Mode
Data Hold Time	tHD,DATA	250	-	ns	normal mode
		100	-		High Speed Mode
		50	-		Ultra High Speed Mode
Data validity time	tVDDAT	-	3.45	µs	normal mode
		-	0.9		High Speed Mode
		-	0.45		Ultra High Speed Mode
response time	tVDACK	-	3.45	µs	normal mode
		-	0.9		High Speed

					Mode
		-	0.45		Ultra High Speed Mode
Bus Load Capacitance	Cload	-	400	pF	normal mode
		-	400		High Speed Mode
		-	550		Ultra High Speed Mode
Bus Pull-up Resistor	RBUS	-	4.7	KΩ	-

3 Pin Definitions

3.1 Pinouts

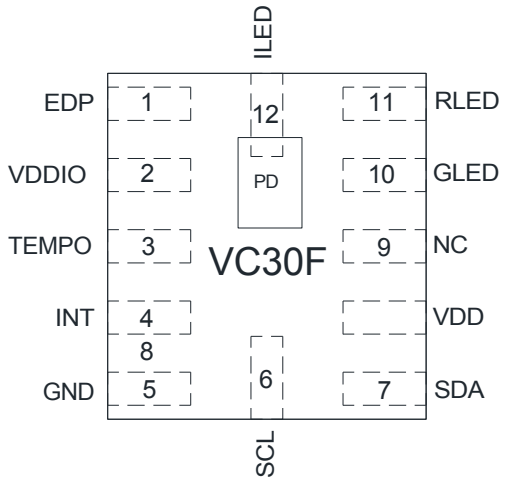


Figure 3-1 VC30F Chip Pin Diagram (Top View)

3.2 Pin Definitions

Table 3-1 VC30F Chip Pin Definitions and Descriptions

Pin Number	Pin Name	clarification
1	EDP	Live Detection Input Pin
2	VDDIO	IO Port Power, 100nF to ground
3	TEMPO	Temperature current output pin, connect NTC to ground, can be grounded or floated if not connected to NTC.
4	INT	interrupt output
5	GND	POWER GROUND
6	SCL	IIC Clock Signal
7	SDA	IIC data lines
8	VDD	AFE Supply, 100nF to Ground
9	NC	--
10	GLED	Green lamp driver pin, connect to green lamp cathode
11	RLED	Red light driver pin, connect to red light cathode
12	ILED	IR driver pin, connect to IR cathode

4 interactive interface

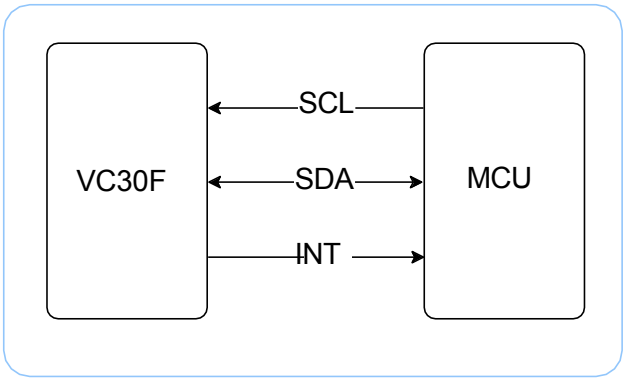


Figure 4-1 VC30F

Connection with Master

Control Table 4-1 VC30F

Connection Pins with

Master Control

pinout	clarification
SCL	IIC clock up to 1MHz
SDA	IIC7-bit device address is 0x33
INT	Interrupt IO without pull-up

- The VC30F supports IIC access and the IIC supports up to 1MHz clock. 7-bit device address of the IIC is 0x33.
- When the VC30F needs data interaction, it sends an interrupt signal to the master through the INT pin.

5 Typical Application Block Diagram

5.1 Typical Application Circuit

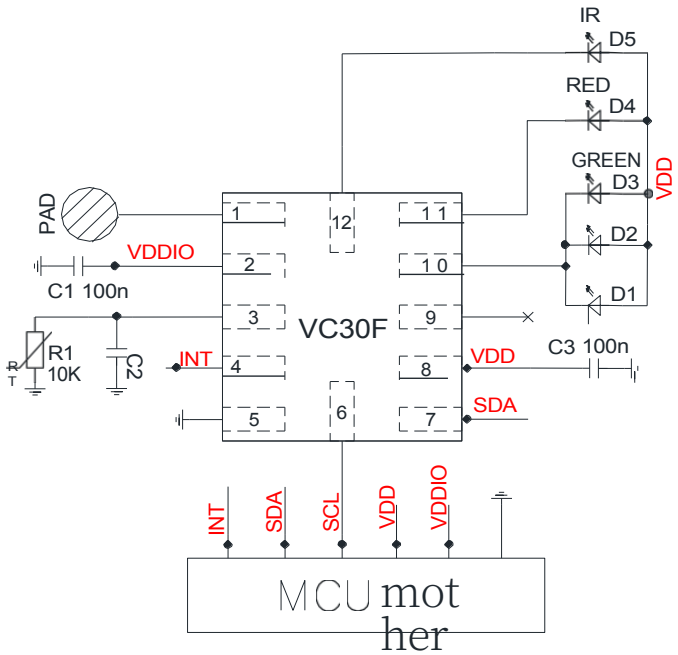


Figure 5-1 VC30F Recommended Circuit Diagram

Decoupling capacitors C1 and C3 are placed as close as possible to the corresponding pins of the VC30F when placed on the PCB; it is recommended to configure a combination of 10uF and 100nF capacitors at the LDO output side of the heart rate board to increase the stability of the heart rate operation.

TEMPO pin (PIN3) is the output pin of constant current source, which can be configured with 4 current stops: 4μA, 8μA, 16μA, 32μA; R1 selects the appropriate resistance value according to the required test temperature range, and C2 calculates the required capacitance value according to the resistance value of R1: $\tau = R1C2<50\mu S$; e.g., R1=10K, C2=2.2nF.

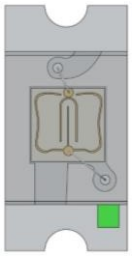
D1, D2, D3 are our super bright green LEDs:

VLG0603H; D4 is our super bright red LED:

VLR0603H;

D5 is our super bright infrared LED: VLI0603H.

When our LEDs are viewed from the outside, the green dots indicate the positive direction of the LEDs, as shown in the figure below for example, VLG0603H:



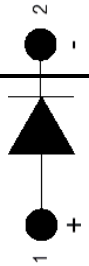
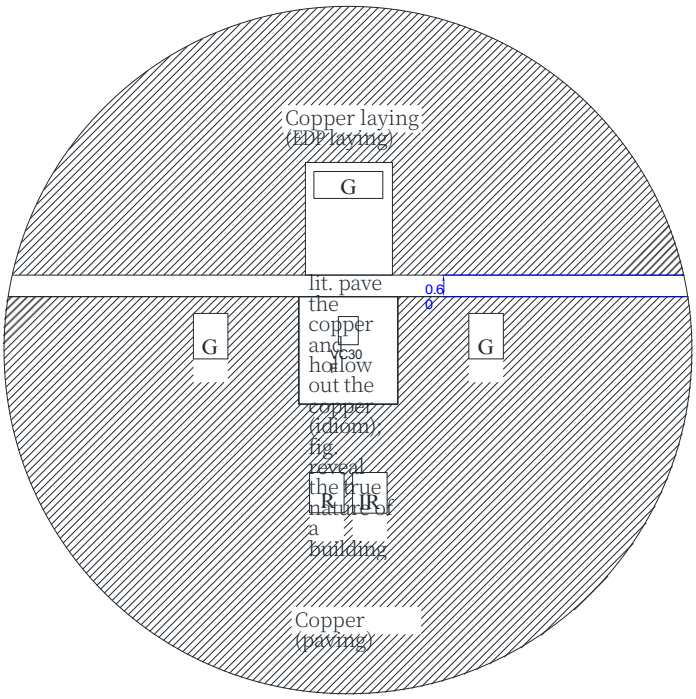


Figure 5-2 VLG0603H Diagram

Figure 5-3 LED Pinout Diagram

PAD adopts top layer copper laying method and connects to the EDP foot, in order to make the effect of vivisection reach the standard, the copper laying area of PAD should be as large as possible, the minimum area should not be lower than 40mm². around the copper laying of EDP, copper laying excavation area should be set up, and the distance should be more than 0.5mm, try to avoid the copper laying of other networks as well as routing, as shown in the following Fig. 5-4 and Fig. 5-5.

If the FPC board needs to be reinforced, it is better to use FR4 material for



reinforcement, if the reinforcement is made of steel, it cannot be grounded.

Figure 5-4 Copper Laying Requirements (Top Layer)

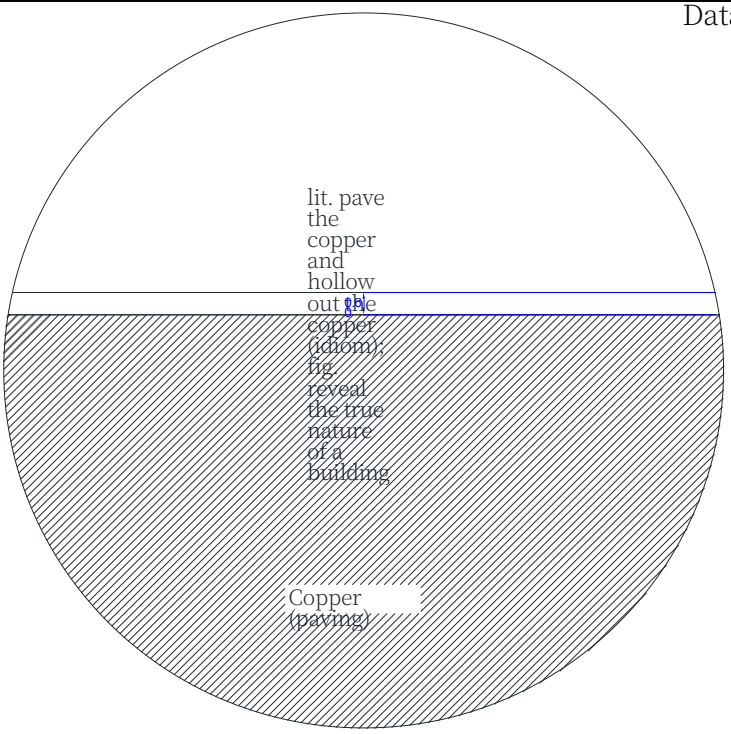


Figure 5-5 Copper Layer Requirements (Bottom Layer)

5.1.1 Power Supply Selection

VC30F chip system power supply involves VDD, VDDIO two-way power supply, the chip's power supply by a LDO for power supply, and the LDO can be freely controlled off. The following power supply methods are recommended:

Table 5-1 Power Supply Information

power supply	Supply Voltage	clarification
VDD	3.3V	● Typical supply voltage for analog and digital power supplies is 3.3V, requiring a peak-to-peak power supply ripple of less than 40mV. ● VDD must go through a decoupling circuit and then be supplied to the IC.
VDDIO	1.8-3.3V	● To match the communication level, the DVDD and VDDIO supply voltages are the same, and the power supply can be shorted and combined.

※Note: VDD and VDDIO can not be powered down alone; heart rate oximetry and wear detection, LED light will require a larger current, the power supply needs to have a better load capacity, and transient response to meet the design requirements. That is, the peak ripple of the LDO output power supply should be less than 40mV, and PSRR should be greater than or equal to 65dB when the output current is 50mA at 1KHz; in addition, the red, and when the current instantly cha ization time of the LDO should be less t op should be less than 100mV.

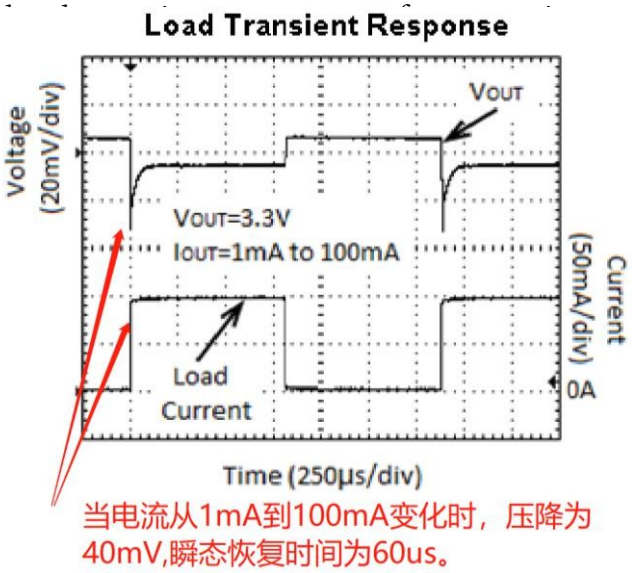


Figure 5-6 LDO Transient Response Reference

5.1.2 Power-Up Timing

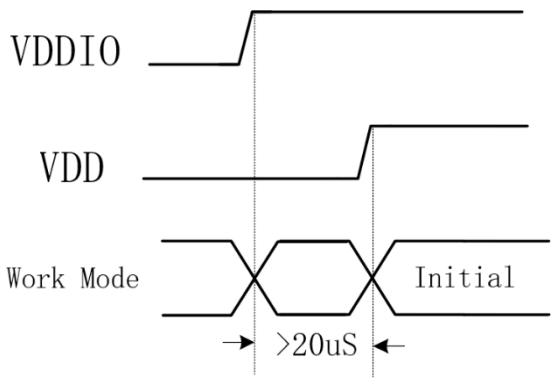


Figure 5-7 Chip Power-Up Timing

5.1.3 reset (a dislocated joint, an electronic device etc)

The chip contains two reset sources: power-on reset POR and software reset. It is recommended to use an LDO with an enable pin for power-on reset.

Table 5-2 Notes on Power Supply

serial number	reset source	clarification
1	Power-on reset	The VC30F can be triggered into operation when the VDD voltage rises to the chip's predetermined POR threshold.
2	software reset	Reset operation can be performed by sending a software reset command to the chip through the communication interface.

5.2 Light Barrier Accessories Description

VC30F and LEDs need to be completely isolated from each other. Customers can refer to the structural design specification for their own design and use of light-isolating materials. It is recommended to use light barrier foam for this solution.

5.3 Recommended Optical Design

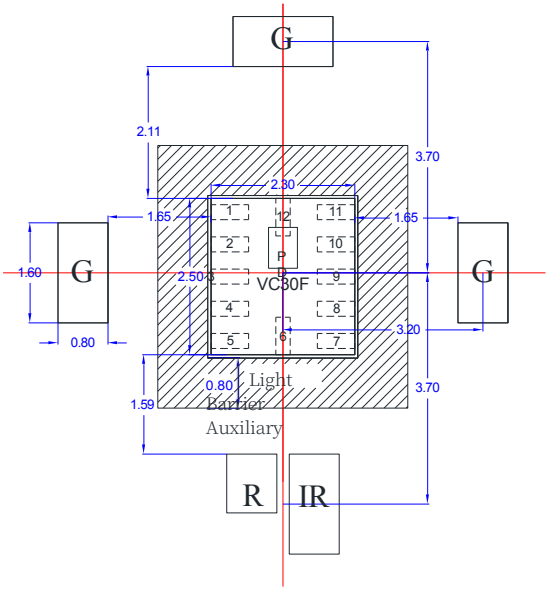


Figure 5-8 VC30F Light Path Layout and Dimensions

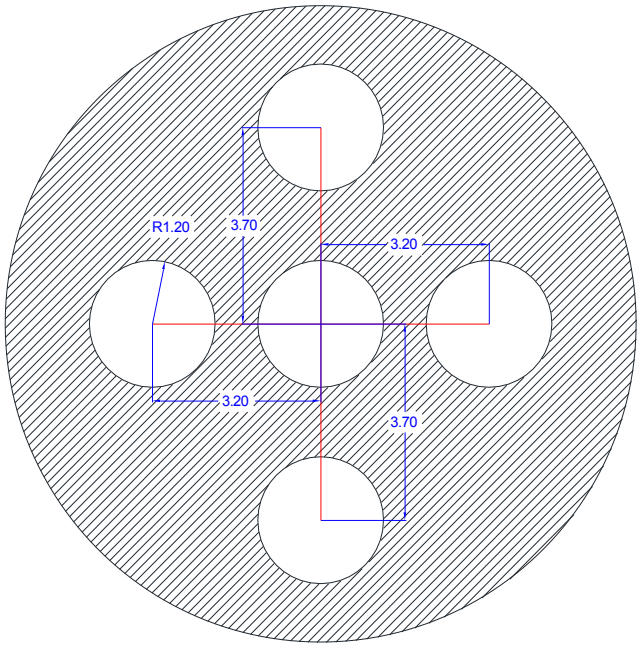


Figure 5-9 VC30F Silkscreen Window Dimensions

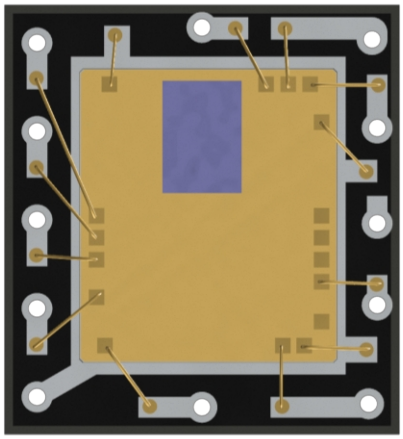
The LED shown in Figure 5-8 above is in the 0603 package and the shaded area around the IC is the light barrier material. Figure 5-9 shows the schematic of the window. Please refer to the structural design specification for detailed requirements.

G for super bright green VLG0603H, IR for super bright infrared VLI0603H, R for super bright red VLR0603H.

6 Package Outside Dimensions

6.1 Package Schematic

The VC30F is packaged in an OLGA package and is schematically shown below.



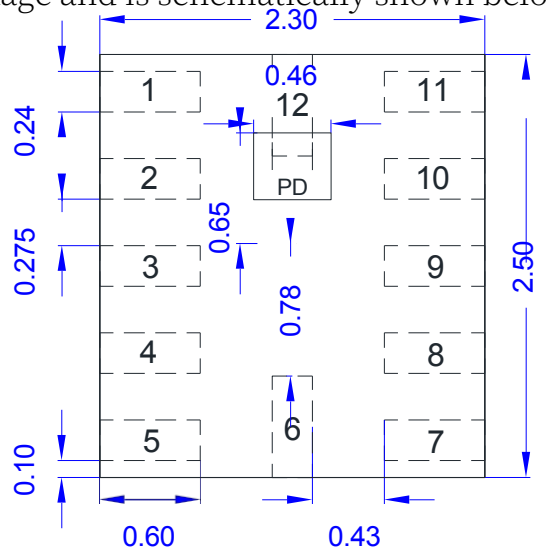


Figure 6-1 Package Top View Schematic (2.3*2.5*0.6mm (±0.1mm))

Recommended pad design PasteMask size and pad size is the same, SolderMask increase 0.1mm on one side, recommended for heart rate ICs.

The Pad parameters are as follows:

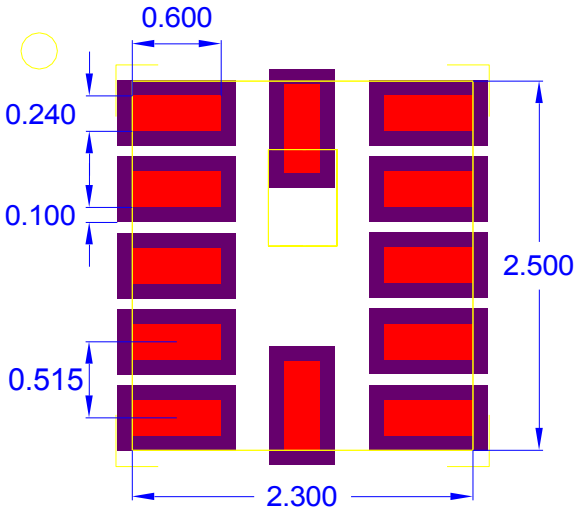


Figure 6-2 Welding Pad Schematic (Unit: mm)

7 Packaging Information and Description of Moisture Sensitivity Levels

VC30F is packaged on tape and reel, 3k/tray, VC30F has a moisture sensitivity level of 3 (MSL3) is packaged in a moisture-proof bag under vacuum with desiccant and humidity indicator card, and is able to be stored in the factory for up to 12 months without being unpacked.

The devices do not require special storage conditions under the following conditions:

- Maintained at a temperature of ≤25°C and relative humidity of ≤50% R.H;
- Maximum temperature of the reflow process should not exceed 255°C.

8 SMT回 Flow Soldering Requirements

8.1 Lead Free回 Flow Curve Schematic Description

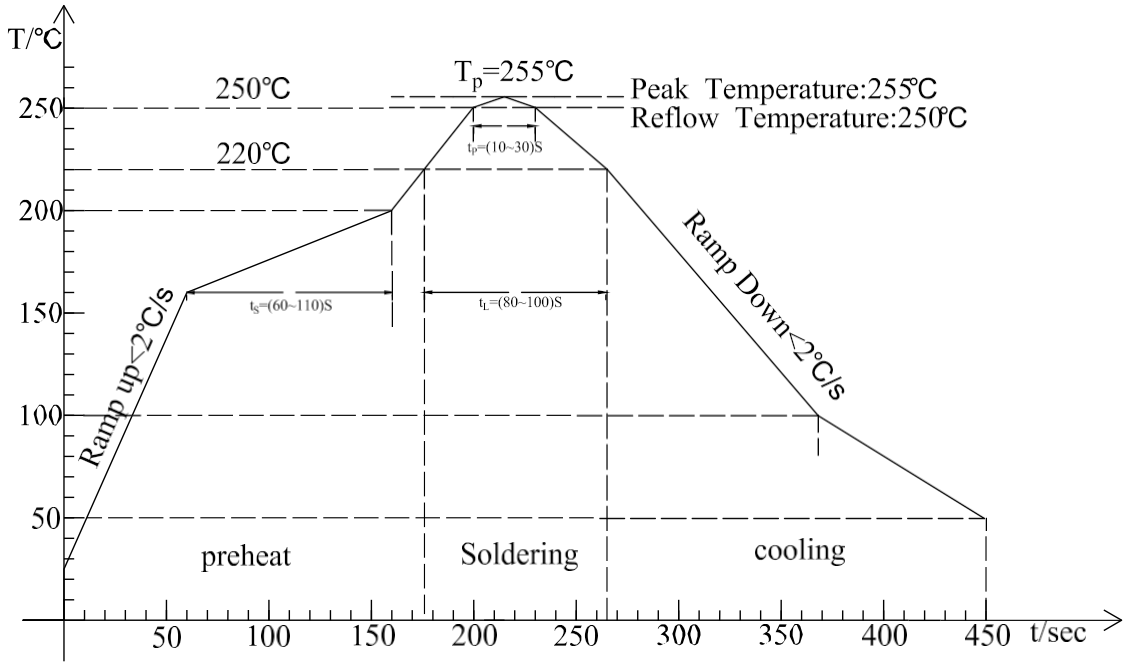


Figure 8-1 Recommended回 Flow Soldering Temperature Profile

9 revised record

releases	dates	revision
V1.0.0	2022/11/27	The official version is released to the public for the first time
V1.0.1	2023/01/17	Modify EDP Recommended Copper Area Size
V1.0.2	2023/02/02	Modify Recommended Circuit LED Model Description
V1.0.3	2023/02/09	Modifying TEMPO Pin Descriptions

10 Contact Information

Vcare

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